L Number	Hits	Search Text	DB	Time stamp
5	26	"5740347"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 23:41
6	6	"5629858"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:17
7	49	"5553008"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:17
8	190	((((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)) and FET and RAM) and feedback	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:46
9	42	(((((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)) and FET and RAM) and feedback) and (716/$.ccls. or 365/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:47
-	364293	transist$4 same circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:47
-	416303	memory same circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:48
-	69983	(transist$4 same circuit) and (memory same circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:50
-	73501	circuit near4 configuration	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:50
-	9741	((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:51
-	461	(((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)) and FET and RAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 18:14
-	190	((((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)) and FET and RAM) and feedback	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:45

L Number	Hits	Search Text	DB	Time stamp
5	26	"5740347"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 23:41
6	6	"5629858"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:17
7	49	"5553008"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:17
-	364293	transist$4 same circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:47
-	416303	memory same circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:48
-	69983	(transist$4 same circuit) and (memory same circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:50
-	73501	circuit near4 configuration	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:50
-	9741	((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 17:51
-	461	(((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)) and FET and RAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/22 18:14
-	190	((((transist$4 same circuit) and (memory same circuit)) and (circuit near4 configuration)) and FET and RAM) and feedback	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/23 00:15

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☒	☐	US 20020015331 A1	20020207	8	Circuit configuration for reading and writing information at a memory cell field	365/189.05
2	☒	☐	US 20010043486 A1	20011122	10	Asymmetric ram cell	365/154
3	☒	☐	US 6487127 B2	20021126	8	Circuit configuration for reading and writing information at a memory cell field	365/189.05
4	☒	☐	US 6484296 B1	20021119	18	Electrical rules checker system and method for reporting problems with tri-state logic in electrical rules checking	716/5
5	☒	☐	US 6484295 B1	20021119	17	Electrical rules checker system and method providing quality assurance of tri-state logic	716/4
6	☒	☐	US 6405347 B1	20020611	27	Method and apparatus for determining the maximum permitted and minimum required width of a feedback FET on a precharge node	716/4
7	☒	☐	US 6363006 B1	20020326	10	Asymmetric RAM cell	365/154
8	☒	☐	US RE37593 E	20020319	179	Large scale integrated circuit with sense amplifier circuits for low voltage operation	365/189.09
9	☒	☐	US 6305003 B1	20011016	24	System and method for propagating clock nodes in a netlist of circuit design	716/12
10	☒	☐	US 6301691 B1	20011009	22	System and method for detecting NFETs that pull up to VDD and PFETs that pull down to ground	716/5
11	☒	☐	US 6240009 B1	20010529	10	Asymmetric ram cell	365/154
12	☒	☐	US 6188641 B1	20010213	19	Synchronous semiconductor memory device having input circuit with reduced power consumption	365/233

	U	1	Document ID	Issue Date	Pages	Title	Current OR
13	☒	☐	US 5889694 A	19990330	19	Dual-addressed rectifier storage device	365/105
14	☒	☐	US 5838630 A	19981117	36	Integrated circuit device, semiconductor memory, and integrated circuit system coping with high-frequency clock signal	365/233
15	☒	☐	US 5793680 A	19980811	35	Input buffer circuit, integrated circuit device, semiconductor memory, and integrated circuit system coping with high-frequency clock signal	365/189.05
16	☒	☐	US 5784291 A	19980721	159	CPU, memory controller, bus bridge integrated circuits, layout structures, system and methods	716/10
17	☒	☐	US 5734919 A	19980331	162	Systems, circuits and methods for mixed voltages and programmable voltage rails on integrated circuits	713/300
18	☒	☐	US 5732246 A	19980324	22	Programmable array interconnect latch	716/16
19	☒	☐	US 5671150 A	19970923	21	System and method for modelling integrated circuit bridging faults	716/4
20	☒	☐	US 5663918 A	19970902	43	Method and apparatus for detecting and selecting voltage supplies for flash memory	365/226
21	☒	☐	US 5644548 A	19970701	81	Dynamic random access memory having bipolar and C-MOS transistor	365/230.06
22	☒	☐	US 5615142 A	19970325	70	Analog memory system storing and communicating frequency domain information	365/45

	U	1	Document ID	Issue Date	Pages	Title	Current OR
23	☒	☐	US 5596522 A	19970121	35	Homogeneous compositions of microcrystalline semiconductor material, semiconductor devices and directly overwritable memory elements fabricated therefrom, and arrays fabricated from the memory elements	365/113
24	☒	☐	US 5592494 A	19970107	20	Current reduction circuit for testing purpose	714/733
25	☒	☐	US 5526313 A	19960611	172	Large scale integrated circuit with sense amplifier circuits for low voltage operation	365/205
26	☒	☐	US 5483486 A	19960109	40	Charge pump circuit for providing multiple output voltages for flash memory	365/185.17
27	☒	☐	US 5465058 A	19951107	30	Graphics system including an output buffer circuit with controlled Miller effect capacitance	326/83
28	☒	☐	US 5406509 A	19950411	32	Electrically erasable, directly overwritable, multibit single cell memory elements and arrays fabricated therefrom	365/113
29	☒	☐	US 5384730 A	19950124	59	Coincident activation of pass transistors in a random access memory	365/156
30	☒	☐	US RE34797 E	19941122	18	Semiconductor memory device having a back-bias voltage generator	365/189.09

	U	1	Document ID	Issue Date	Pages	Title	Current OR
31	☒	☐	US 5365126 A	19941115	31	Graphics system including an output buffer circuit with controlled Miller effect capacitance	326/83
32	☒	☐	US 5339275 A	19940816	78	Analog memory system	365/45
33	☒	☐	US 5335219 A	19940802	37	Homogeneous composition of microcrystalline semiconductor material, semiconductor devices and directly overwritable memory elements fabricated therefrom, and arrays fabricated from the memory elements	369/288
34	☒	☐	US 5297097 A	19940322	176	Large scale integrated circuit for low voltage operation	365/226
35	☒	☐	US 5274778 A	19931228	18	EPROM register providing a full time static output signal	365/185.21
36	☒	☐	US 5262999 A	19931116	167	Large scale integrated circuit for low voltage operation	365/226
37	☒	☐	US 5193198 A	19930309	13	Method and apparatus for reduced power integrated circuit operation	327/536
38	☒	☐	US 4931675 A	19900605	NA	Semiconductor sense amplifier	327/55
39	☒	☐	US 4910706 A	19900320	NA	Analog memory for storing digital information	365/45
40	☒	☐	US 4445189 A	19840424	NA	Analog memory for storing digital information	708/1

	U	1	Document ID	Issue Date	Pages	Title	Current OR
41	☒	☐	US 4403308 A	19830906	NA	Apparatus for and method of refreshing MOS memory	365/222
42	☒	☐	US 4322819 A	19820330	NA	Memory system having servo compensation	365/45